What is claimed is:

1. A multimode spread spectrum receiver with a shared circuitry operation, capable of receiving at least two types of code division multiple access (CDMA) signals, comprising:

an antenna, responsive to a radio frequency signal containing said at least two types of code division multiple access (CDMA) signals, for providing a radio frequency electrical signal;

a preprocessor, responsive to the radio frequency electrical signal, for providing a digital signal; and

at least one multimode receiving channel block, responsive to the digital signal and selecting, based on a predetermined selection criteria, one of at least two types of coding corresponding to one of said at least two types code division multiple access (CDMA) signals and utilizing said coding for further processing of said digital signal by said at least one multimode receiving block using said shared circuitry operation.

2. The multimode receiver of claim 1, wherein the digital signal is a digital intermediate frequency signal, wherein said selection is performed by the at least one multimode receiving channel block in response to a mode selection signal or to a mode-generating selection signal and wherein said at least one multimode receiving channel block generates, based on said selection, and provides internally one of the at least two code signals to said at least one multimode receiving channel block for implementing said further processing.

3. The multimode receiver of claim 2, wherein the at least one multimode receiving channel block is further responsive to a code control signal and providing a code and carrier measurement signal.

4. The multimode receiver of claim 3, further comprising:

a receiver processing block, responsive to the code and carrier measurement signal, for providing the code control signal, a frequency control signal, and the mode selection signal or the mode-generating selection signal.

5. The multimode receiver of claim 4, further comprising:

a residual carrier removing block, responsive to the digital intermediate frequency signal, for providing a data intermediate signal; and

an integration and dumping block responsive to the data intermediate signal, to said one of the at least two code signals, for providing P dump signals to the receiver processing block, wherein P is an integer of at least a value of one.

6. The multimode receiver of claim 4, wherein the at least one multimode receiving channel block comprises:

a code numerically controlled oscillator block, responsive to the code control signal, for providing a numerically controlled oscillator clock signal;

a first code generator, responsive to the numerically controlled oscillator clock signal, for providing a first one of the at least two code signals for a corresponding first one of the at least two types of the code division multiple access receiver processing;

a second code generator responsive to the numerically controlled oscillator clock signal, for providing a second one of the at least two code signals for a corresponding second one of the at least two types of the code division multiple access receiver processing; and

a code selector, responsive to the mode selection signal, to said first one of the at least two code signals and to said second one of the at least two code signals, for providing said first one of the at least two code signals or said second one of the at least two code signals, selected by the code selector based on the mode selection signal, for further processing by the at least one multimode receiving channel block using said shared circuitry operation.

7. The multimode receiver of claim 6, wherein the first code generator, the second code generator or both code generators contain binary offset carrier capabilities.

8. The multimode receiver of claim 6, wherein the first one of the at least two code signals is for global positioning system receiver processing and the second one of the at least two code signals is for Galileo receiver processing.

9. The multimode receiver of claim 2, wherein the at least one multimode receiving channel block comprises:

a code numerically controlled oscillator block responsive to the code control signal, for providing a numerically controlled oscillator clock signal; and

a universal code generator, responsive to the numerically controlled oscillator clock signal and to the mode-generating selection signal, for generating and providing, based on the mode-generating selection signal, a first one of the at least two code signals for a corresponding first one of the at least two types of the code division multiple access receiver processing or a second one of the at least two code signals for a corresponding second one of the at least two types of the code division multiple access receiver processing for further processing by the at least one multimode receiving channel block using said shared circuitry operation.

10. The multimode receiver of claim 9, wherein the universal code generator contains binary offset carrier capabilities.

11. The multimode spread spectrum receiver of claim 1, wherein said receiver is a multimode global navigation satellite system receiver.

12. The multimode receiver of claim 11, wherein a first one of the at least two code signals is for global positioning system receiver processing and a second one of the at least two code signals is for Galileo receiver processing.

13. A method for a shared circuitry operation of a multimode spread spectrum receiver, capable of receiving at least two types of code division multiple access signals, comprising:

receiving the radio frequency signal containing said at least two types of code division multiple access signals by an antenna of the multimode spread spectrum

receiver and converting said radio frequency signal to a radio frequency electrical signal;

converting the radio frequency electrical signal to a digital signal by a preprocessor of the multimode spread spectrum receiver and providing said digital signal to the at least one multimode receiving channel block; and

selecting by at least one multimode receiving channel block, based on a predetermined selection criteria, one of at least two types of coding corresponding to one of said at least two types code division multiple access signals and utilizing said coding for further processing of said digital signal by said at least one multimode receiving block using said shared circuitry operation.

14. The method of claim 13, wherein the digital signal is a digital intermediate frequency signal, wherein said selection is performed by the at least one multimode receiving channel block in response to a mode selection signal or to a mode-generating selection signal and wherein said at least one multimode receiving channel block generates, based on said selection, and provides internally one of the at least two code signals to said at least one multimode receiving channel block for implementing said further processing.

15. The method of claim 14, wherein said selection by at least one multimode receiving block, based on a predetermined selection criteria, of one of at least two types of coding comprises:

generating a first one of the at least two code signals for a corresponding first one of the at least two types of the code division multiple access receiver processing by a first code generator and generating a second one of the at least two code signals for a corresponding second one of the at least two types of the code division multiple access receiver processing by a second code generator and providing said first one of the at least two code signals and said second one of the at least two code signals to a code selector of the at least one multimode receiving channel block, wherein said first one of the at least two code signals and said second one of the at least two code signals are parts of said at least one multimode receiving channel block;

selecting said first one of the at least two code signals or said second one of the at least two code signals by the code selector; and

providing the selected said first one of the at least two code signals or said second one of the at least two code signals for further processing by the at least one multimode receiving channel block using said shared circuitry operation.

16. The method of claim 15, wherein said selecting of said first one of the at least two code signals or said second one of the at least two code signals by the code selector is based on the mode selection signal provided to the code selector by a receiver processing block.

17. The method of claim 15, wherein before generating the first one of the at least two code signals and the second one of the at least two code signals, the method further comprises:

providing a code control signal to a code numerically controlled oscillator block of the at least one multimode receiving channel block; and

generating, in response to said code control signal, a numerically controlled oscillator clock signal by the code numerically controlled oscillator block and providing the numerically controlled oscillator clock signal to the first code generator and to the second code generator.

18. The method of claim 17, wherein said code control signal is provided to the code numerically controlled oscillator block by a receiver processing block.

19. The method of claim 15, wherein the further processing is performed by an integrating and dumping block of the at least one multimode receiving channel block.

20. The method of claim 19, wherein before providing the code control signal, the method further comprises:

generating a data intermediate signal by removing a residual carrier frequency from the digital intermediate frequency signal by a residual carrier removing block of the at least one multimode receiving channel block and providing said data intermediate signal to the integrating and dumping block for further processing.

21. The method of claim 14, wherein said selection by at least one multimode receiving block, based on a predetermined selection criteria, of one of at least two types of coding comprises: generating a first one of the at least two code signals for a corresponding first one of the at least two types of the code division multiple access receiver processing or a second one of the at least two code signals for a corresponding second one of the at least two types of the code division multiple access receiver processing by a universal code generator of the at least one multimode receiving channel block; and

providing the first one of the at least two code signals or the second one of the at least two code signals by the universal code generator for further processing by the at least one multimode receiving channel block using said shared circuitry operation.

22. The method of claim 21, wherein generating the first one of the at least two code signals or the second one of the at least two code signals by the universal code generator is based on the mode-generating selection signal provided to the universal code generator by a receiver processing block.

23. The method of claim 21, wherein before generating the first one of the at least two code signals and the second one of the at least two code signals, the method further comprises:

providing a code control signal to a code numerically controlled oscillator block of the at least one multimode receiving channel block; and

generating, in response to said code control signal, a numerically controlled oscillator clock signal by the code numerically controlled oscillator block and providing the numerically controlled oscillator clock signal to the universal code generator.

24. The method of claim 21, wherein said code control signal is provided to the code numerically controlled oscillator block by a receiver processing block.

25. The method of claim 21, wherein the further processing is performed by an integrating and dumping block of the at least one multimode receiving channel block.

26. The method of claim 25, wherein before providing the code control signal, the method further comprises:

generating a data intermediate signal by removing a residual carrier frequency from the digital intermediate frequency signal by a residual carrier removing block of the at least one multimode receiving channel block and providing said data intermediate signal to the integrating and dumping block for further processing.

27. The method of claim 13, wherein said receiver is a multimode global navigation satellite system receiver.

28. The method of claim 27, wherein a first one of the at least two code signals is for global positioning system receiver processing and a second one of the at least two code signals is for Galileo receiver processing.

29. A computer program product comprising: a computer readable storage structure embodying computer program code thereon for execution by a computer processor with said computer program code, characterized in that it includes instructions for performing the steps of the method of claim 13 indicated as being performed by the multimode spread spectrum receiver, or by the multimode receiving channel block of said spread spectrum receiver, or by a terminal containing said spread spectrum receiver.

30. A system for communicating at least two types of code division multiple access signals received by a multimode spread spectrum receiver with a shared circuitry operation, comprising:

at least one satellite, for providing said at least two types of code division multiple access signals, or at least two satellites each providing one of said at least two types of the code division multiple access signals;

at least one base station, for providing said at least two types of the code division multiple access signals used for mobile communications; and

a terminal, responsive to said at least two different types of the code division multiple access signals, wherein said terminal containing said multimode spread spectrum receiver capable of receiving said at least two types of code division

multiple access signals using at least one multimode receiving channel block, responsive to the digital signal indicative of one of said at least two different types of the code division multiple access signals and selecting, based on a predetermined selection criteria, one of at least two types of coding corresponding to said one of the at least two types code division multiple access signals and utilizing said coding for further processing of said digital signal by said at least one multimode receiving block using said shared circuitry operation.

31. A multimode receiving module with a shared circuitry operation capable of receiving at least two types of code division multiple access signals and contained in a multimode spread spectrum receiver, comprising:

at least one multimode receiving channel block, responsive to the digital signal containing one of said at least two types of the code division multiple access signals and selecting, based on a predetermined selection criteria, one of at least two types of coding corresponding to said one of at least two types code division multiple access signals and utilizing said coding for further processing of said digital signal by said at least one multimode receiving block using said shared circuitry operation,

wherein said multimode receiving module is removable from said multimode spread spectrum receiver.